AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An insulated-gate field-effect transistor, comprising:

first and second impurity regions placed so as to oppose each other;

a strained silicon layer having a channel between both the first and second impurity regions;

a gate insulator placed at least in a region corresponding to the channel, on top of the strained silicon layer; and

a gate electrode on top of the gate insulator,

wherein a region of the strained silicon layer, corresponding to the channel, does not have a silicon germanium layer in contact therewith, and ~~the strained silicon layer, in~~ regions of the strained silicon layer, other than the region corresponding to the channel, ~~have regions where~~ do have the silicon germanium layer [[is]] in contact therewith.

2. (currently amended) An insulated-gate field-effect transistor according to Claim 1, wherein a source electrode and a drain electrode, in contact with the first and second impurity regions, respectively, each include regions of the [[a]] silicon germanium layer in contact with the strained silicon layer.

3. (currently amended) An insulated-gate field-effect transistor according to Claim 1, wherein the strained silicon layer is placed in [[the]] an upper part of a substrate and the silicon germanium layer is not present ~~does not exist~~ in the region of the strained silicon layer, corresponding to ~~at least~~ the channel, and on a side adjacent to the substrate.

4. (currently amended) An insulated-gate field-effect transistor according to Claim 1, wherein the strained silicon layer is placed in [[the]] an upper part of a substrate and a void ~~exists~~ is disposed in a region on a side adjacent to the substrate, opposite from a face portion of the strained silicon layer[[,]] corresponding to at least the channel.

5. (currently amended) An insulated-gate field-effect transistor according to Claim 1, wherein the

strained silicon layer is placed in [[the]] an upper part of a substrate and an insulating film ~~exists in a region~~ is disposed on a side adjacent to the substrate, opposite from a face portion of the strained silicon layer[[,]] corresponding to ~~at least~~ the channel.

6. (original) An insulated-gate field-effect transistor according to Claim 1, wherein a portion of the region of the strained silicon layer, corresponding to the channel, does not have a silicon germanium layer in contact therewith.

7. (currently amended) A semiconductor device, comprising: ~~having an~~

a first insulated-gate field-effect transistor comprising:

first and second impurity regions placed so as to oppose each other;

a strained silicon layer having a channel between both the first and second impurity regions;

a gate insulator placed at least in a region corresponding to the channel, on top of the strained silicon layer; and

a gate electrode placed on top of the gate insulator,

wherein a region of the strained silicon layer, corresponding to the channel, does not have a silicon germanium layer in contact therewith, and ~~the strained silicon layer, in~~ regions of the strained silicon layer, other than the region corresponding to the channel, do have ~~regions where~~ the silicon germanium layer ~~is~~ in contact therewith, and

a second ~~an~~ insulated-gate field-effect transistor comprising:

first and second impurity regions placed so as to oppose each other;

a strained silicon layer having a channel between both the first and second impurity regions;

a gate insulator placed at least in a region corresponding to the channel, on top of the strained silicon layer; and

a gate electrode placed on top of the gate insulator, wherein a portion of a region of the strained silicon layer, corresponding to the channel, does not have a silicon germanium layer in contact therewith; and

wherein said first and second insulated-gate field-effect transistors ~~being~~ are formed on the same support substrate.

8. (currently amended) An insulated-gate field-effect transistor, comprising:

a support substrate;

a bar-shaped strained silicon layer on the support substrate;

a gate insulator formed so as to spread across [[the]] an upper surface of the bar-shaped strained silicon layer, in [[the]] a direction orthogonal to [[the]] a longitudinal direction of the bar-shaped strained silicon layer, and ~~thereof~~, covering at least a part of both sides of the bar-shaped strained silicon layer;

a gate electrode formed on the gate insulator; and

a source region and a drain region, placed in regions positioned on opposite sides of the gate electrode, respectively, and along the longitudinal direction of the bar-shaped strained silicon layer,

wherein a channel is formed in a portion of the bar-shaped strained silicon layer, corresponding to a region on the underside of the gate electrode, in such a way as to extend along the longitudinal direction of the bar-shaped strained silicon layer.

9. (currently amended) An insulated-gate field-effect transistor according to claim 8, wherein the gate

electrode is formed on the gate insulator on the sides of two faces of the bar-shaped strained silicon layer, ~~intersecting the support substrate and~~ extending along the longitudinal direction of the bar-shaped strained silicon layer~~, respectively~~.

10. (currently amended) An insulated-gate field-effect transistor according to claim 8, having a silicon germanium layer in contact with the bar-shaped strained silicon layer at opposite ends of the bar-shaped strained silicon layer, in the longitudinal direction thereof and under a region where the channel does not exist[[s]].

11. (currently amended) An insulated-gate field-effect transistor according to claim 8, wherein a plurality of the bar-shaped strained silicon layers are provided and ~~a set of~~ the source region and the drain region ~~is~~ are formed such that the source region and the drain region are common to the plurality of the bar-shaped strained silicon layers, and are connected to a plurality of channels.

12. (currently amended) An insulated-gate field-effect transistor, comprising:

a support substrate;

a plurality of bar-shaped strained silicon layers disposed with longitudinal sides thereof, opposed to each other, on the support substrate;

a plurality of bar-shaped silicon germanium layers each disposed between adjacent layers of the plurality of the bar-shaped strained silicon layers;

a gate insulator formed so as to spread across the longitudinal sides of the plurality of the bar-shaped strained silicon layers[[;]] and the plurality of the bar-shaped silicon germanium layers;

a plurality of gate electrodes formed on the gate insulator; and

a source region and a drain region, formed in regions on opposite sides of the respective gate electrodes, respectively, and along the longitudinal direction of the plurality of the bar-shaped strained silicon layers~~,~~ and the plurality of the bar-shaped silicon germanium layers,

wherein a plurality of channels is formed in regions of the plurality of the bar-shaped strained silicon layers, corresponding to the undersides of the respective gate electrodes, and on the side away from the support substrate.

13. (currently amended) An insulated-gate field-effect transistor according to Claim 12, wherein ~~a~~ the

plurality of channels ~~is~~ are formed on the sides of two faces of the respective bar-shaped strained silicon layers, along the direction intersecting the support substrate, respectively.

14. (currently amended) An insulated-gate field-effect transistor according to Claim 12, wherein the source region and drain region are connected to a plurality of channel regions ~~common to~~ and the plurality of the bar-shaped strained silicon layers, respectively.

15. (original) An insulated-gate field-effect transistor according to Claim 8, wherein the support substrate is a substrate the top surface of which has direction of crystal plane (100), and the longitudinal direction of the bar-shaped strained silicon layer is substantially parallel to a direction <100> of the support substrate.

16. (original) An insulated-gate field-effect transistor according to Claim 11, wherein the support substrate is a substrate the top surface of which has direction of crystal plane (100), and the longitudinal direction of the bar-shaped strained silicon layers is

substantially parallel to a direction <100> of the support substrate.

17. (original) An insulated-gate field-effect transistor according to Claim 8, wherein the support substrate is a substrate the top surface of which has direction of crystal plane (100), and the longitudinal direction of the bar-shaped strained silicon layer is substantially parallel to a direction <110> of the support substrate.

18. (original) An insulated-gate field-effect transistor according to Claim 11, wherein the support substrate is a substrate the top surface of which has direction of crystal plane (100), and the longitudinal direction of the bar-shaped strained silicon layers is substantially parallel to a direction <110> of the support substrate.

19. (currently amended) A method of fabricating an insulated-gate field-effect transistor, comprising the steps of:

preparing a silicon substrate;

forming an oxide film on the surface of the silicon substrate;

defining an opening by etching a portion of the oxide film;

implanting ions into the opening;

causing silicon germanium seed crystals to grow in the opening;

depositing amorphous silicon germanium on top of the opening and the oxide film;

heating the amorphous silicon germanium to ~~be turned into~~ create silicon germanium crystals; and

depositing a strained silicon layer on top of the silicon germanium crystals.

20. (currently amended) A method of fabricating an insulated-gate field-effect transistor, comprising the steps of:

preparing a silicon substrate;

forming an oxide film on the surface of the silicon substrate;

defining an opening by etching a portion of the oxide film;

causing silicon germanium seed crystals to grow in the opening;

oxidizing [[the]] surfaces of the silicon germanium seed crystals;

subjecting the silicon germanium seed crystals to high-temperature heat treatment;

removing [[an]] oxide film on the surfaces of the silicon germanium seed crystals;

depositing amorphous silicon germanium on top of the opening and the oxide film;

heating the amorphous silicon germanium to ~~be turned into~~ create silicon germanium crystals; and

depositing a strained silicon layer on top of the silicon germanium crystals.